數位電路設計 (資工一)

**Spring, 2022**

**\* 2-hour in-person/on-site class and 1-hour/2-hour asynchronous on-line class per week**

**(每週 兩小時實體課程 + 一或兩小時非同步線上課程)**

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| 週次  Week | 日期  Date | 預定進度  Planned Schedule | 實際進度  Actual Progress |
| 1 | **2/16 (三) 34** | **2/16 No Class (停課一日)(校慶活動)**Syllabus課程綱要, Ch1 (Ch1: Digital Systems and Binary Numbers) | On-line class (線上視訊上課):  **No Class (停課一日)(校慶活動)**  Google meet: <https://meet.google.com/wsu-mbhr-hxy>  提供想加選本課程的同學試聽，初步了解本課程進行方式及討論加選相關事宜 (Preliminary understanding of how this course is conducted and the matters related to adding the course) |
| Asynchronous On-line Class | Course Video (課程錄影): e3  p.1-1~1-73  (§1-1 ~ §1-9) |
| 2 | 2/23 (三) 34 | Ch1, Ch2 (Ch2: Boolean Algebra and Logic Gates) | On-line class (線上視訊上課):  Google meet: <https://meet.google.com/wsu-mbhr-hxy>  說明課程綱要、複習上週課程內容、討論提問、講授本週課程內容  Syllabus, Review of the course contents for the previous week, Q&A, Lecture of the course contents for this week |
| Asynchronous On-line Class | Course Video (課程錄影): e3  p.2-1~2-49  (§2-1 ~ §2-5) |
| 3 | 3/2 (三) 34 | Ch2, Lab0說明  Lab#0 announcement (?/?) | In-person class (實體課程): **EC122** **Quiz#1** |
| Asynchronous On-line Class | Course Video (課程錄影): |
| 4 | 3/9 (三) 34 | Ch2, Ch3  (Ch3: Gate-Level Minimization) | In-person class (實體課程): **Quiz** |
| Asynchronous On-line Class | Course Video (課程錄影): |
| 5 | 3/16 (三) 34 | Ch3  Lab#0 due (?/?) | In-person class (實體課程): **Quiz** |
| Asynchronous On-line Class | Course Video (課程錄影): |
| 6 | **3/23 (三) 34** | **Exam#1**  Ch3, Lab1說明  Lab#1 announcement (?/?) | In-person class (實體課程):  **Exam#1**  **時間：**  **地點：**  **範圍：** |
| Asynchronous On-line Class | Course Video (課程錄影): |
| 7 | 3/30 (三) 34 | Ch4  (Ch4: Combinational Logic) | In-person class (實體課程): |
| Asynchronous On-line Class | Course Video (課程錄影): |
| 8 | **4/6 (三) 34** | **4/6 Holiday (放假一天)**  Ch4 | In-person class (實體課程):  **Holiday (放假一天)** |
| Asynchronous On-line Class | Course Video (課程錄影): |
| 9 | 4/13 (三) 34 | Ch4, Ch5  (Ch5: Synchronous Sequential Logic)  **HW of Exam#1 (?/?)**  **Lab#1 due (?/?)** | In-person class (實體課程): **Quiz** |
| Asynchronous On-line Class | Course Video (課程錄影): |
| 10 | 4/20 (三) 34 | Ch5, Lab2說明  Lab#2 announcement (?/?) | In-person class (實體課程): **Quiz** |
| Asynchronous On-line Class | Course Video (課程錄影): |
| 11 | **4/27 (三) 34** | **Exam#2 5/5 (三) CD**  Ch5 | In-person class (實體課程):  **Exam#2**  **時間：**  **地點：**  **範圍：** |
| Asynchronous On-line Class | Course Video (課程錄影): |
| 12 | 5/4 (三) 34 | Ch5, Lab3說明  Ch6  (Ch6: Registers and Counters)  Lab#3 announcement (?/?) | In-person class (實體課程): |
| Asynchronous On-line Class | Course Video (課程錄影): |
| 13 | 5/11 (三) 34 | Ch6  **Lab#2 due (?/?)**  **Lab#2 Demo (?/?)** | In-person class (實體課程): **Quiz** |
| Asynchronous On-line Class | Course Video (課程錄影): |
| 14 | 5/18 (三) 34 | Ch6  Ch7  (Ch7: Memory and Programmable Logic)  **HW of Exam#2 (?/?)** | In-person class (實體課程): **Quiz** |
| Asynchronous On-line Class | Course Video (課程錄影): |
| 15 | 5/25 (三) 34 | Ch7  **Lab#3 due (?/?)**  **Lab#3 Demo (?/?)** | In-person class (實體課程): **Quiz** |
| Asynchronous On-line Class | Course Video (課程錄影): |
| 16 | **6/1 (三) 34** | **Exam#3 6/9 (三) CD** | **Exam#3:**  **時間：**  **地點：**  **範圍：** |
| x | x |
| 17 |  | **彈性補充教學**  **Lab#3 due (?/?)**  **Lab#3 Demo (?/?)** | **彈性補充教學** |
| 18 |  | **彈性補充教學** | **彈性補充教學** |

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| Chapter  Semester | 1  (+Syllabus) | 2  (+Lab0) | 3  (+Lab1) | 4  (+Lab2) | 5  (+Lab3) | 6 | 7 | Exam &  檢討考卷 | 放假 |
| 2018 Spring | 5 | 7 | 8 | 8 | 10 | 5 | 3 | 3+3+3+2 | 7 |
| 2019 Spring | 5 (4+1) | 7 (6+1) | 7 (5.5+1.5) | 9 (6+3) | 9 (7+2) | 5 | 3 | 3+3+3+2 | 3 |
| 2020 Spring | 6 | 5 | 8 | 9 (6+3) | 8 (6+2) | 5 | 4 | 2+2+2+2 | x |
| 2020 Summer | 5 | 7 | 8 | 8 | 9 | 5 | 4 | 3+3+3+2 | x |
| 2021 Spring | 5 | 8 | 8 | 10 |  |  |  | 3+3+3+2 |  |

Verilog code simulator:

1. ModelSim

2. EDA Playground

<https://eda-playground.readthedocs.io/en/latest/intro.html>

3. iVerilog (compiler) + gtkwave (simulator) ⇒ Icarus Verilog + GTKWave

<http://inf-server.inf.uth.gr/~konstadel/resources/Icarus_Verilog_GTKWave_guide.pdf>